This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

1. (Currently Amended) A method for implementing at speed bit fail mapping of an embedded memory system having BIST (Built In Self Testing), comprising:

_____using a high speed multiplied clock which is a multiple of an external clock of a tester to sequence BIST bit fail testing of the embedded memory system, said BIST generating a fail map data for capture by a diagnostic register device;

_____pausing the BIST testing upon recognition of a fail of the embedded memory system;

_____using the external clock of the tester to read bit fail data out from said diagnostic register device to the tester;

_____resuming the BIST testing with the high speed multiplied clock from the point at which it was paused.

2. (Original) The method of claim 1, used for bit fail mapping of an embedded DRAM (Dynamic Random Access Memory).

3. (Original) The method of claim 2, including using an on-chip clock multiplier to multiply the external clock to generate the high speed multiplied clock.

4. (Currently Amended) The method of claim 3, including using the on-chip clock multiplier to multiply the external clock of an off-chip ATE (Automatic Test Equipment) tester to generate the high speed multiplied clock. [[.]]

5. (Currently Amended) The method of claim 4, including storing the location of the fail in fail location latches of said diagnostic register device upon recognition of the fail, and using logic that pauses the BIST testing and also de-gates a functional clock to the fail location registers, allowing the bit fail data to be shifted off the chip from said diagnostic register device to the ATE tester.

6. (Original) The method of claim 5, further including using a multiplexer having a first input from the tester clock and a second input from the high speed multiplied clock, and the logic causes the multiplexer to pass either the first input from the tester clock or the second input from the high speed multiplied clock.

7. (Currently Amended) A method for high speed bit fail mapping of an embedded circuit having BIST (Built In Self Testing) by a tester having a tester clock with minimal interaction from the tester, comprising:

_____running the BIST testing off an internal multiplied clock of the tester clock for BIST testing;

_____pausing the BIST testing upon recognition of a fail, said BIST generating a fail map data for capture by a diagnostic register device;

the tester directing a handshake signal to the BIST testing when the tester is available to capture bit fail mapping data; and,

transferring said fail map data from said diagnostic register device to said tester.

8. (Original) The method of claim 7, used for bit fail mapping of an embedded DRAM (Dynamic Random Access Memory).

9. (Original) The method of claim 8, including using an on-chip clock multiplier to multiply the external clock to generate the high speed multiplied clock.

10. (Currently Amended) The method of claim 9, including using the on-chip clock multiplier to multiply the external clock of an off-chip ATE (Automatic Test Equipment) tester to generate the high speed multiplied clock. [[.]]

11. (Currently Amended) The method of claim 10, including storing the location of the fail in fail location latches of said diagnostic register device upon recognition of the fail, and using logic that pauses the BIST testing and also de-gates a functional clock to the fail location registers, allowing the bit fail data to be shifted off the chip from said diagnostic register device to the ATE tester.

12. (Original) The method of claim 11, further including using a multiplexer having a first input from the tester clock and a second input from the high speed multiplied clock, and the logic causes the multiplexer to pass either the first input from the tester clock or the second input from the high speed multiplied clock.

13. (Currently Amended) A circuit for implementing at speed bit fail mapping of an embedded memory system having a BIST (Built In Self Testing) engine on a chip, comprising:

_____an off-chip tester having a tester clock;

_____the BIST engine using a high speed multiplied clock which is a multiple of the tester clock to sequence the BIST engine for bit fail testing of the embedded memory system, said BIST engine generating a fail map data for capture by a diagnostic register device;

_____the circuit including logic for pausing the BIST testing upon recognition of a fail of the embedded memory system, using the tester clock to read bit fail data out to the tester, and thereafter resuming the BIST testing with the high speed multiplied clock from the point at which BIST testing was paused.

14. (Original) The circuit of claim 13, for automatic bit fail mapping of an embedded DRAM (Dynamic Random Access Memory), including an on-chip clock multiplier for multiplying the tester clock of an off-chip ATE (Automatic Test Equipment) tester to produce the high speed multiplied clock, wherein the logic pauses the BIST engine at a point when a mismatch between BIST expected data and the actual data read from the DRAM is encountered, then shifts the bit fail data off the chip using the low-speed ATE tester clock, and then resumes the BIST engine using the high speed multiplied clock to provide an at speed bit fail map.

15. (Currently Amended) The circuit of claim 14, including fail location latches for storing the location of the fail upon recognition of the fail, and the logic that stops the BIST engine also de-gates a functional clock to the fail location registers, allowing the bit fail data to be shifted off the chip from said diagnostic register device to the ATE tester.

16. (Original) The circuit of claim 15, further comprising a multiplexer having a first input from the tester clock and a second input from the high speed multiplied clock, and the logic causes the multiplexer to pass either the first input from the tester clock or the second input from the high speed multiplied clock to the BIST engine.

17. (Currently Amended) A circuit enabling at speed bit fail mapping of an embedded memory system, the circuit comprising:

_____a bit fail map data register having diagnostic latches used to store data on failing memory locations for the generation of a bit fail map;

_____a first control latch that asserts a pause signal upon receiving a fail data signal indicating a mismatch comparison between expected data from the embedded memory system and actual data read from the embedded memory system;

_____a second control latch that is set upon receiving the pause signal from the first control latch and asserts a shift ~~enble~~ enable signal to enable a shift out of the data on failing memory locations from the bit fail map data register for the generation of a bit fail map.

18. (Currently Amended) The circuit of claim 17, wherein the pause signal of the first control latch pauses test circuitry for testing the embedded memory system and enables a continue/handshake signal from an external tester to enable the second control latch to asserts the shift ~~enble~~ enable signal to enable a shift out of the data on failing memory locations from the bit fail map data register for the generation of a bit fail map.

19. (Original) The circuit of claim 18, wherein the first and second control latches include both master latches, which are clocked with function data with a function clock or with scan data with a scan clock, and slave latches which are updated with master latch data with a slave latch clock.

20. (Original) The circuit of claim 19, for automatic bit fail mapping of an embedded DRAM (Dynamic Random Access Memory), including an on-chip clock multiplier for multiplying the tester clock of an off-chip ATE (Automatic Test Equipment) tester to produce the high speed multiplied clock, wherein logic which includes the first and second control latches pauses a BIST (Built In Self Testing) engine at a point when a mismatch between BIST expected data and the actual data read from the DRAM is encountered, then shifts the bit fail data off the chip using the low-speed ATE tester clock, and then resumes the BIST engine using the high speed multiplied clock to provide an at speed bit fail map.

21. (Original) The circuit of claim 20, wherein the bit fail map data register includes fail location latches for storing the location of the fail upon recognition of the fail, and the logic that stops the BIST engine also de-gates a clock to the fail location registers, allowing the bit fail data to be shifted off the chip to the ATE tester.

22. (Original) The circuit of claim 21, further comprising a multiplexer having a first input from the tester clock and a second input from the high speed multiplied clock, and the logic causes the multiplexer to pass either the first input from the tester clock or the second input from the high speed multiplied clock to the BIST engine.

23. (New) The method of claim 1, wherein new fail map data can be captured on every high speed multiplied clock cycle.

24. (New) The method of claim 7, wherein new fail map data can be captured on every high speed multiplied clock cycle.

25. (New) The circuit of claim 13, wherein new fail map data can be captured on every high speed multiplied clock cycle.